ABSTRACT OF THE DISCLOSURE

The delay locked loop ("DLL") delay interval can be locked to stop the DLL from wasting power in unnecessarily switching to synchronize the device with the DLL is associated to the system clock. This is achieved by adding logic sensing when a DRAM device will not imminently be called upon to output data and when the device has stabilized. Waiting for the DLL delay interval to stabilize before locking the delay interval still allows the DLL to immediately and effectively resume operations when the DLL is needed to synchronize the output of the DRAM device with the system clock. The DLL delay interval can be locked, together with the DLL clock, after the DRAM device is deselected by the chip select control line, after a number of no operation commands have been received, and/or after any command issued to the DRAM device has been completed.